AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions, and listings, of claims in the captioned patent application.

Listing of Claims

1. (Currently Amended) A source synchronous link comprising:

a communication link;

a source synchronous receiver coupled to said communication link; [[and]]

a source synchronous transmitter coupled to said communication link, ~~including~~ comprising:

data transmit logic configured to manage the transmission of data signals over at least one [[a]] data line of said communication link; and

data strobe transmit logic configured to generate [[a]] one or more data strobe signals over a corresponding one or more clock ~~lines~~ line of said communication link, wherein said data strobe transmit logic halts each said one or more data strobe signals in a selected logical state in response to an external condition.

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2. (Currently Amended) The source synchronous link of claim 1, wherein said one or more data strobe signals comprise a first data strobe signal and a second data strobe signal transmitted with a phase opposite a phase of said first ~~frequency~~ data strobe signal.

3. (Original) The source synchronous link of claim 1, wherein said first data strobe signal and said second data strobe signal may be transmitted at either one of two logical states and wherein said data strobe transmit logic maintains said first data strobe signal at a first of said two logical states and maintains said second data strobe signal at a second of said two logical states when said data strobe transmit logic halts said one or more data strobe signals.

4. (Currently Amended) A source synchronous transmitter constructed and arranged to transmit [[a]] differential data strobe signals over a source synchronous communication link at a first frequency, with the differential data strobe signals

toggling between one of two logical states at said first frequency when operating in a normal mode of operation and with the differential data strobe signals held at one of the logical states when operating in a data capture debug mode of operation.

5. (Canceled)

6. (Currently Amended) The source synchronous link of claim 4, wherein said transmitter comprises:

~~a differential~~ data strobe transmit logic configured to generate said ~~differential~~ at least one data strobe as a differential data strobe comprising a data strobe signal and an inverse data strobe signal[[:]] ; said data strobe transmit logic comprising:

a differential data strobe signal generator configured to determine ~~a said~~ logical ~~states~~ levels of said data strobe signal and said inverse data strobe ~~signals~~ signal;

[[a]] strobe stopping logic that controls a plurality of ~~said~~ logic level signals utilized by said signal generator to cause said data strobe and said inverse data strobe signals to remain halted in a desired logical state.

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7-10. (Canceled)

11. (Currently Amended) A differential data strobe transmitter for ~~generating~~ transmitting over a source synchronous communication link a differential data strobe comprising a data strobe signal and an inverse data strobe signal ~~over a communication link~~ with a data signal, comprising:

a differential data strobe signal generator that determines a shape of said data strobe signal and said inverse data strobe signal waveforms; and

strobe stopping logic configured to control signal level states used by said signal generator logic to cause said data strobe signal and said inverse data strobe signal to remain halted in a desired ~~logical~~ state.

12. (Currently Amended) The differential data strobe transmitter of claim 11, wherein said differential data strobe signal generator ~~logic~~ selects alternately between two applied signal levels to generate each said data strobe signal and said inverse data strobe signal.

13. (Original) The differential data strobe transmitter of claim 12, wherein said differential data strobe signal generator receives a s inputs a first and a second logic level signal for selection to generate said data strobe signal and a third and fourth logic level signals for selection to generate said inverse data strobe signal.

14. (Currently Amended) The differential data strobe transmitter of ~~claim 12~~ claim 13,

wherein during normal operations, said differential data strobe is not halted, said first and third input signals are held consistently in an asserted state while said second of fourth input signals are held consistently in a de-asserted state, and

wherein said signal generator selects alternately said first and said second input signals to generate said data strobe signal at a first clock frequency, and between said third and said fourth input signals to generate said inverse data strobe signal at said first clock frequency.

15. (Original) The differential data strobe transmitter of claim 12, wherein said data strobe signal and said inverse data strobe signal are each generated as single ended bits that are opposite in phase with each other.